United States District Court
For the Northern District of California

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IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

COMPUTER CACHE COHERENCY CORPORATION, Plaintiff, v. VIA TECHNOLOGIES, INC. and VIA TECHNOLOGIES, INC. (USA), Defendants.	No. C-05-01668 RMW ORDER ON CROSS-MOTIONS RE: INFRINGEMENT **[Re Docket No. 96, 101, 105, 107, 109 and 220]**
COMPUTER CACHE COHERENCY CORPORATION, Plaintiff, v. INTEL CORPORATION, Defendant.	No. C-05-01766 RMW ORDER ON CROSS-MOTIONS RE: INFRINGEMENT AND INTEL'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY **[Re Docket No. 76 and 150]**

Defendant Intel Corporation ("Intel") seeks summary judgment that U.S. Patent No. 5,072,369 ("the '369 patent") is invalid as anticipated or obvious in light of prior art references.

The parties have also filed cross-motions for summary judgment with respect to infringement of the '369 patent. Specifically, plaintiff Computer Cache Coherency Corporation ("CCCC") seeks summary judgment that defendants' accused products literally infringe claim 1 of the '369 patent, the only claim asserted by CCCC.[1] Defendants Via Technologies, Inc. and Via Technologies, Inc. (USA) (collectively, "Via") and Intel seek summary judgment of non-infringement with respect to claim 1. After the court issued its claim construction order, CCCC sought and was granted leave to submit supplemental briefing on two claim terms for which the court did not adopt either side's proposed construction, "bus" and "SNOOP signal." The court granted CCCC's motion to submit supplemental briefing and permitted defendants to submit an opposition to that supplemental briefing ("Supp. Br. I.").

Thereafter, CCCC moved on December 10, 2007 for leave to file an amended complaint in *CCCC v. Intel*, Case No. 05-01766, to add new Intel products that have allegedly been made, sold, offered for sale and used after the filing of the original complaint. At a hearing on April 11, 2008, the court tentatively granted CCCC's motion to amend the complaint, permitted each side to take one deposition and asked the parties to agree to a date on which their experts were available to answer questions by the court. The court permitted the parties to file yet further supplemental briefing ten days in advance of the agreed-upon hearing date ("Supp. Br. II"). The parties appeared on August 20, 2008, with their experts: Dr. Michel Dubois for CCCC and Dr. John Levy for Intel. Via made available a corporate representative for the court's questions but largely relied upon Intel's expert's positions.

The court has considered the parties' papers as well as the oral arguments and evidence on the summary judgment motions presented in conjunction with the claim construction hearing and at the technical expert hearing. For the reasons discussed below, the court denies CCCC's motions for summary judgment of literal infringement as to Intel and Via. The court grants Via's motion for summary judgment of non-infringement, but denies Via's motion for summary judgment based on the license agreement with AMD. The court also grants Intel's motion for summary judgment of

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[1] CCCC does not seek summary judgment that Intel or Via's products infringe under the doctrine of equivalents.

non-infringement, but denies without prejudice Intel's motion for summary judgment of invalidity of the '369 patent. Finally, the court denies CCCC's motion to amend its complaint to add additional Intel products.

I. BACKGROUND

CCCC moves for summary judgment that both defendants' accused products literally infringe claim 1 of the '369 patent; Via and Intel move for summary judgment of non-infringement, both literally and under the doctrine of equivalents.

A. '369 Patent

CCCC owns by assignment the '369 patent. It has sued defendants Via in one action for infringing claim 1 of the '369 patent and defendant Intel for infringing the same claim in another action. These two actions have been consolidated for purposes of claim construction and related summary judgment motions.

The '369 patent discloses an interface circuit that permits devices connected to two different buses to utilize a main memory on one of the two buses, where the main memory on that bus has a cache memory. Computer systems may maintain a copy of some of the information stored in main memory in a cache memory to permit faster computer operation. Data in cache memory can be updated without a corresponding update to memory, resulting in the data in memory becoming stale. When this occurs, the cache and main memory are non-coherent.

The invention purports to solve, in the context of two buses, a "cache coherency" problem wherein a device requesting data from memory that has been cached is able to access the most current data in memory, whether that data is stored in main memory or in cache memory.

CCCC asserts only claim 1 of the '369 patent in this action. Claim 1 reads:

An apparatus for providing data communication between first and second buses,

> the first bus providing a first plurality of bus masters connected thereto with data read and write access to first data storage locations mapped to separate addresses within a first address space, wherein one of said first plurality of bus masters writes data to a first particular one of said first data storage locations by placing on the first bus an address to which the first particular one of said first data storage locations is mapped and transmitting the data via said first bus, and wherein one of said first plurality of bus masters reads data from a second particular one of said first data storage locations by placing on the first bus an address to which the second particular one of said first storage locations is mapped and receiving data via said first bus,

> the second bus providing a second plurality of bus masters connected thereto with data read and write access to second data storage locations mapped to separate addresses within a second address space, wherein one of said second plurality of bus masters writes data to a first particular one of said second data storage locations by placing on the second bus an address to which the first particular one of said second data storage locations is mapped and transmitting the data via said second bus, and wherein one of said second plurality of bus masters reads data from a second particular one of said second data storage locations by placing on the second bus an address to which the second particular one of said second storage locations is mapped and receiving data via said second bus,
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> wherein one of said second plurality of bus masters connected to said second bus caches data read out of a subset of said second data storage locations, said second bus including means for conveying a SNOOP signal with an address appearing on the bus, the SNOOP signal telling said one of said second plurality of bus masters when to write cached data to the address appearing on the bus,
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> the apparatus comprising:
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> first mapping means coupled to said first bus for mapping first addresses within the first address space to second addresses within the second address space, for asserting an indicating signal and for generating one of said second addresses in response to one of said first addresses transmitted on said first bus from one of said first plurality of bus masters, said first mapping means also generating a SNOOP signal of a state indicating when a generated second address is mapped to one of said particular subset of the second data storage locations, and
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> bus interface means connected to said first and second buses for responding to the first indicating signal when said one of said first plurality of bus masters is reading data by placing the generated second address and SNOOP signal on the second bus, receiving data from a second data storage location mapped to said second address, and transmitting the received data to said one of said first plurality of bus masters via said first bus when the said one of said first plurality of bus masters is reading data.

'369 patent at 12:42-14:21. Claim 1 of the '369 patent claims an apparatus for providing data communications between two buses, referred to in the specification as an interface circuit, comprising a mapping means and a bus interface means. These limitations are set forth in the last two paragraphs of the claim. Claim 1 also includes a three-paragraph preamble. The first paragraph of the preamble describes the attributes of the first bus; the second and third paragraphs of the preamble describe the attributes of the second bus.

Part of the mechanism described in the '369 patent for solving the cache coherency problem is the snoop operation. In general, a snoop operation checks a cache memory to determine whether a memory address and the data associated with the memory address are in cache. Deposition of Jeffrey L. Rabe ("Rabe Dep.") 64:15-18. Much of the parties' dispute involves how the preamble limits claim 1 and whether or how snoop operations are performed in the accused products.

B. Claim Construction

The parties agree on the construction of three terms:

Term	***Agreed Construction***
"mapped"	"Established correspondence between the elements of one set and elements of another set."
"bus master"	"A device or system which is capable of initiating or controlling bus transactions."
"address"	"An identification, such as a label, number, or name that designates a particular location in storage or any other data destination or source."

The court construed the following terms in its Order on Claim Construction and Associated Motion for Summary Judgment of Invalidity Based on Indefiniteness, Docket No. 138 ("Claim Construction Order"):

Term	***Court's Construction***
"bus"	"A signal line or set of signal lines used by an interface system to connect a number of devices and to transfer information between the devices."
"address space", "first address space", "second address space"	"A set of addresses." "First address space" is an address space that necessarily refers to addresses represented on the first bus; "second address space" is an address space that necessarily refers to addresses represented on the second bus.
"SNOOP signal"	"A signal indicating whether an address references a cached data storage location."
"the SNOOP signal telling said one of said second plurality of bus masters when to write cached data to the address appearing on the bus"	"The SNOOP signal indicating to one of the bus masters on the second bus when to write cached data to the one of the second data storage locations at the address appearing on the second bus."
"a SNOOP signal of a state indicating when a generated second address is mapped to one of said particular subset of the second data storage locations"	(no construction necessary)
"said second bus including means for conveying a SNOOP signal with an address appearing on the bus"	"A second bus with the function of conveying a SNOOP signal with an address appearing on the bus and having the structure of a Futurebus or its equivalents."
"mapping"	"Establishing a correspondence between the elements of one set and elements of another set."
"mapping first addresses within the first address space to second addresses within the second address space"	(no construction necessary)
"first mapping means"	Function: (1) mapping the first addresses to second addresses, (2) asserting an indicating signal, (3) generating a second address in response to a first address transmitted on the first bus from a first bus master, and (4) generating a SNOOP signal. Structure: the V-F translation circuit 18 and address generator 47 and equivalents thereof.

Term	*Court's Construction*
"indicating signal"	"V-LREQ request signal" which is a signal that requests control of the first bus.
"responding to the first indicating signal when said one of said first plurality of bus masters is reading data by placing the generated second address and SNOOP signal on the second bus"	"Responding to the indicating signal when one of the bus masters connected to the first bus is reading data by placing the generated second address and SNOOP signal on the second bus."
"bus interface means"	Function: (1) responding to the first indicating signal when a first bus master reads data by placing the generated second address and SNOOP signal on the second bus, (2) receiving data from a memory on the second bus, and (3) transmitting the received data to a first bus master. Structure: buffer **22**, buffer **49**, buffer **24**, buffer **36**, local data buses **14** and **16**, buffer **32**, and Futurebus arbitration and control circuit **40** and equivalents thereof.

C. The Accused Products

CCCC has accused Intel and Via chipsets of infringing the '369 patent. The term chipset is commonly used to refer to a pair of specialized chips on a computer's motherboard. A chipset acts as a "traffic cop," managing the interactions between a computer's processor (or CPU), memory, and peripheral devices. Intel produces motherboard chipsets for its own line of processors; Via produced[2] motherboard chipsets for processors made by Intel and Advanced Micro Devices ("AMD").

In chipsets, one of the chips is generally referred to as the Northbridge, the other is referred to as the Southbridge. In Intel systems, the Northbridge is also referred to as the memory controller hub or "MCH"; the Southbridge is also referred to as the I/O controller hub or "ICH." In both Intel and AMD chipsets, the Northbridge is directly connected to the processor and generally handles communications between the processor, main memory (or DRAM) and peripherals requiring high-speed access such as accelerated graphics cards ("AGP") that connect directly to the computer's motherboard. The Southbridge, by contrast, is not directly connected to the processor and typically handles a computer's input/output ("I/O") functions, including peripherals, audio and slower graphics functions. Although a chipset manages their interactions, it does not itself include a processor, memory or peripherals.

[2] Via contends that it is no longer in the chipset business with respect to Intel and AMD processors.

1. Accused Intel Chipsets

CCCC has accused chipsets from Intel's Desktop, Laptop, Mature, Server and Workstation product lines of infringing claim 1 of the '369 patent. All of these Intel chipsets include an MCH (the Northbridge) and an ICH (the Southbridge). CCCC also seeks to amend its complaint to add approximately 40 other Intel lines of chipsets as accused devices. These chipsets were apparently brought to market after CCCC filed its complaint on April 28, 2008. As discussed further below, five of those new chipsets, Intel's 5000p, 5000v, 5000x, 54000 and 7300 lines of chipsets operate differently from other chipsets in that they incorporate a feature called a "snoop filter." In general, the MCH and ICH are connected to one another through a Direct Media Interface ("DMI") connection, referred to by Intel as a hub link interface. Declaration of Jeffrey Rabe ("Rabe Decl.") ¶ 5; Rabe Dep. 45:6-15.

As set forth above, the Northbridge handles communications between the processor, main memory and high-speed peripherals (lower-speed peripherals are typically handled by the Southbridge). Host processors such as Intel Pentium processors, which may have cache memories, are connected to the chipset via the front side bus; the front side bus is directly connected to the Northbridge. Rabe Decl. ¶ 7; Rabe Dep. 95:13-15. System memory connects to the Northbridge via a separate dedicated memory bus.

The Southbridge connects to several components, including Universal Serial Bus ("USB") and Peripheral Component Interconnect ("PCI") devices. For example, connected to the Southbridge is a PCI bus that may support multiple PCI devices (or, as the patent refers to them, bus masters). *Id.* ¶ 6. Rabe Dep. 21:13-15. PCI is an industry-standard bus protocol used in connecting peripheral devices such as computer audio cards to a computer motherboard. Rabe Decl. ¶ 6.

The chipset processes and routes transactions between the various devices connected to the Northbridge and Southbridge to the front side bus or memory bus to obtain the requested data. The chipset then returns the data to the requesting device.

2. Accused Via Chipsets

CCCC has accused Via chipsets that operate with AMD's K7 and K8 processors and Intel's P4 and P3 processors of infringing claim 1 of the '369 patent. It is undisputed that the accused Via

chipsets only work in combination with processors made by Intel or AMD. Decl. Bernard Peuto ("Peuto Decl.") ¶ 46. Via refers to the accused chipsets as "core logic chipsets," the computer components which connect the processor in a personal computer to peripheral devices and other components. A core logic chipset consists of two separate chips that are connected together, a "Northbridge" chip and a "Southbridge" chip. Peuto Decl. ¶ 45. As in the accused Intel chipsets, the Northbridge chip facilitates communication between higher speed devices within the computer such as the processor, main memory and high-speed graphics devices. The Southbridge chip connects slower-speed devices such as the keyboard, mouse and disk drive.

II. ANALYSIS

"Summary judgment is appropriate in a patent case, as in other cases, when there is no genuine issue as to any material fact and the moving party is entitled to judgment as a matter of law." *Nike, Inc. v. Wolverine World Wide, Inc.*, 43 F.3d 644, 646 (Fed. Cir. 1994) (citations omitted). Summary judgment can be used to determine both infringement and non-infringement. *Avia Group Intern., Inc. v. L.A. Gear California, Inc.*, 853 F.2d 1557, 1560 (Fed. Cir. 1988). The moving party bears the burden of proving infringement or non-infringement by a preponderance of the evidence. *Mannesmann Demag Corp. v. Engineered Metal Products, Inc.*, 793 F.2d 1279, 1282 (Fed. Cir. 1986).

To establish infringement, every limitation in a claim as construed by the court must be in the accused product, either exactly or by substantial equivalent. *Carroll Touch, Inc., v. Electro Mech. Sys., Inc.*, 15 F.3d 1573, 1576 (Fed. Cir. 1993). "Literal infringement requires the patentee to prove that the accused device contains each limitation of the asserted claim(s) . . . . If any claim limitation is absent from the accused device, there is no literal infringement as a matter of law." *Bayer AG v. Elan Pharm. Research Corp.*, 212 F.3d 1241, 1247 (Fed. Cir. 2000) (citation omitted). Although an accused product does not literally infringe, it may still be found to infringe under the doctrine of equivalents. *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 21 (1997). Infringement under the doctrine of equivalents is found where the accused product does not literally correspond to the asserted claim but functions in the same way and obtain the same result as the asserted claim. *Graver Tank & Mfg. Co. v. Linde Air Prods. Co.*, 339 U.S. 605, 608 (1950). District

courts are obliged to grant summary judgment "[w]here the evidence is such that no reasonable jury could determine two elements to be equivalent" or where "under the particular facts of a case . . . a theory of equivalence would entirely vitiate a particular claim element." *Warner-Jenkinson*, 520 U.S. at 39 & n.8; *see also DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1016 (Fed. Cir. 2006).

A. Preamble of Claim 1

As an initial matter, defendants and CCCC dispute whether defendants may directly infringe claim 1 of the '369 patent where the accused products do not include certain structure set forth in the preamble of that claim. As the court previously determined in its claim construction order, the preamble is limiting. *See* Claim Construction Order at 4-5.

CCCC argues that the '369 patent claims solely "an apparatus for providing data communications," beginning with the language "the apparatus comprising." It argues that the '369 patent does not claim the combination of the data communications apparatus and two buses, rather only the interface circuit itself. CCCC contends that the presence of the two buses is not required in the accused products in order for those products to infringe, rather, it is only required that the accused products operate in an environment in which two buses meeting the limitations of the preamble are present.

It is permissible for a patentee to draft claims in terms of the environment in which the claimed invention operates. The environment constitutes a limitation of the claimed invention. *See e.g., In re Stencel*, 828 F.2d 751, 754 (Fed. Cir. 1987) ("As a matter of claim draftsmanship, appellant is not barred from describing the driver in terms of the structure imposed upon it by the collar having plastically deformable lobes. The framework – the teachings of the prior art – against which patentability is measured is not all drivers broadly, but drivers suitable for use in combination with this collar, for the claims themselves are so limited."). When considering infringement of such a claim, all of the structure described in the required environment must be present, however, the accused product itself need not itself supply the environment. *See, e.g., In Smith Corona Corp. v. Pelikan, Inc.*, 784 F. Supp. 452, 463 (M.D. Tenn. 1992), *aff'd in unpublished opinion*, 1 F.3d 1252 (Fed. Cir. 1993) ("[P]atentability can be predicated upon how a claimed item mates with another

item without claiming the combination of two items."); *see also Ricoh Co., Ltd. v. Katun Corp.*, 380 F. Supp. 2d 418, 436 (D.N.J. 2005) ("The Court finds that although the preambles of the claims are limitations, the parts described therein are not claimed as a combination with the developer container. . . . The bottle and image forming apparatus mentioned in the preamble describe the environment in which the claimed lid is to be used, but are not claimed in combination with the lid.").[3]

Accordingly, although the court finds that the preamble of claim 1 is limiting, in order to prove direct infringement by defendants, CCCC need not show that the accused chipsets include the two buses and bus masters as described in the preamble. However, because these buses form the environment in which the claimed apparatus operates, CCCC must demonstrate that the accused products operate with buses that include all limitations described in the preamble.

The court thus rejects defendants' arguments that the accused chipsets cannot directly infringe the '369 patent because CCCC has failed to demonstrate that the chipsets themselves include the buses as set forth in the preamble. While defendants may be found not to infringe because their chipsets do not operate in the particular two-bus environment to which the preamble limits the claimed invention, they cannot prove non-infringement merely by demonstrating that the accused chipsets do not themselves include the buses set forth in the preamble.

B. Alleged Infringement by Intel

1. CCCC's Infringement Contentions

CCCC contends that it should be granted summary judgment that the accused Intel chipsets literally infringe the '369 patent. CCCC asserts that the Intel chipsets meet every limitation of claim 1 of the '369 patent. It contends that evidence, uncontradicted by Intel, shows that the Intel chipsets operate in the two-bus environment set forth in the preamble.

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[3] Defendant Intel correctly points out that *Smith Corona* and *Ricoh* do not bind this court. Nevertheless, those courts correctly recognize that a preamble may be limiting, but that the structure set forth in such a preamble need not be present in the accused device where the limitations are present in the environment in which the accused device operates. Intel also contends that the preamble for claim 1 of the '369 patent is significantly longer than the body of the claim and introduces and defines numerous terms set forth in the body of the claim. That the preamble is complex and supplies antecedents necessary to give life to the claim informs whether the preamble is limiting (as the court has decided it is), not necessarily whether the structure of the preamble must be found in the accused device.

Intel asserts that, even assuming that CCCC need not prove that Intel supplies the buses described in the preamble, limitations involving the SNOOP signal and mapping means set forth in the body of claim 1 are not present in the Intel accused products and preclude a grant of summary judgment of literal infringement to CCCC. Intel further cross-moves for summary judgment of non-infringement on the grounds that the accused Intel chipsets lack a SNOOP signal or other signal meeting the limitations of claim 1 that are related to the SNOOP signal.

2. First and Second Buses

As discussed above, one of the threshold disputes between the parties concerns whether CCCC is required to prove that Intel supplies the buses described in the preamble as part of Intel's accused chipset products. The court has concluded that CCCC must prove that the accused chipsets operate in the environment described in the preamble, but not that Intel's accused devices must supply the buses described in the preamble.

The claimed apparatus operates to provide data communication between first and second buses, each bus having the distinct characteristics set forth in the preamble. In support of its literal infringement argument, CCCC asserts that a PCI bus connected to the Southbridge (ICH) of Intel's accused chipsets constitutes the first bus described in the preamble of claim 1. CCCC asserts that front side bus (or host bus) that connects the Northbridge (MCH) of Intel's chipsets to the processor or CPU constitutes the second bus described in the preamble of claim 1.

As with "SNOOP signal" discussed below, the parties continue to disagree about the appropriate construction of "bus." CCCC proposed that bus be construed as "[o]ne or more conductors used for transmitting signals or power from one or more sources to one or more destinations"; defendants proposed that bus be construed as "[a] set of parallel conductors that is capable of transmitting signals between two or more modules (such as computer processors and local memories) connected to those conductors." The court did not adopt either side's proposed construction and instead construed bus as "a signal line or set of signal lines used by an interface system to connect a number of devices and to transfer information between the devices." Claim Construction Order at 8.

CCCC contends that the front side bus connected to all of defendants' accused products is the "second bus" claimed in claim 1. Defendants point out, for example, that in the accused Via chipsets, the front side bus is a point-to-point bus, meaning that it only connects a single source to a single destination. Defendants contend that the court's construction of bus does not include such buses. CCCC, on the other hand, believes that the court's construction of "bus" was meant to include point-to-point as well as shared buses.

As defendants correctly point out, the court's construction is not meant to encompass a bus which only operates as a point-to-point connection. The court expressly stated this when setting forth its reason for its claim construction for bus:

> Upon review of the available IEEE definitions circa 1998, IEEE definition number 2, which relates to a "microcomputer system bus," defines "bus" to be "a signal line or set of lines used by an interface system to connect a number of devices and to transfer information." *See* Salik Decl. (dkt. # 46), Ex. 10. This definition of bus, which describes a shared bus, is more appropriate in light of the claim language. The preamble specifies "the first bus providing a first plurality of bus masters connected thereto", '369 patent at 12:43-4, and "the second bus providing a second plurality of bus masters connected thereto", '369 patent at 12:58-9. It is thus clear from the claim language that the patent contemplates shared buses—buses that are connected to a plurality of bus masters such that the buses connect multiple devices—and not buses that connect a single source to a single destination. Indeed, all uses of "bus" in the claims and the specification of the '369 patent describe a shared structure to which multiple bus masters are connected.

Claim Construction Order at 8. Defendants have correctly interpreted the court's claim construction as requiring a "bus" to connect more than a single source to a single destination.

Based on the evidence and argument presented for purposes of the cross-motions for summary judgment, there did not appear to be any dispute that these buses meet the environmental limitations described in the preamble of claim 1. However, in its supplemental briefing, Intel asserts that "[m]ost of the accused desktop chipsets, and all of the Express and server chipsets CCCC seeks to add to the case . . . implement a dedicated, i.e. 'point to point' front side bus for each CPU that communicates with the MCH." Although this statement does not appear to be disputed by CCCC, the court nevertheless has located no evidence in the record that this is necessarily the case. Thus, the court is unable to determine which of the accused Intel chipsets operate in the required two-bus environment including a first and second *shared* bus meeting the limitations of the first two paragraphs of the preamble of claim 1.

3. SNOOP Signal

Intel bases its motion for summary judgment of non-infringement in large part upon its contention that its accused chipsets do not include a SNOOP signal meeting the limitations of claim 1. Although the court construed the "SNOOP signal" in its Claim Construction Order, the parties continue to disagree over the construction and interpret the court's construction differently.

a. The Parties' Dispute Regarding the Court's Construction

In claim construction briefing, CCCC proposed that SNOOP signal be construed as "a signal that triggers a determination of whether the data corresponding to an address in cacheable memory is cached"; defendants proposed that SNOOP signal be construed as "a signal indicating whether a generated second address references a cached data storage location." The court did not adopt either side's proposed construction and instead construed SNOOP signal as "a signal indicating whether an address references a cached data storage location." Claim Construction Order at 12. In its order, the court rejected CCCC's proposed construction, stating "the SNOOP signal indicates whether an address references a cached storage location, it does not merely trigger a determination whether data is cached." *Id.* at 11.

The parties now disagree on what the court means by "cached data storage location." Defendants contend that the court's use of "cached data storage location" in the construction of "SNOOP signal" means that the SNOOP signal must indicate that data is in fact cached at the referenced location. CCCC, on the other hand, contends that a SNOOP signal indicates whether an address falls within a range of addresses subject to caching (or, to state it more simply, that the address is one that is "cacheable") but that a SNOOP signal need not indicate whether data is actually cached at the referenced data storage location. *See* CCCC Supp. Br. re: MSJs, Docket No. 139-2 at 4 ("CCCC Supp. Br. I") ("[A] 'cached data storage location' says nothing of whether the data itself has been cached; it merely states that a location – a data storage location – is a part of cache memory. In much the same way, a street address might indicate a particular type of home, but does not indicate whether the home is occupied at a particular moment."); CCCC 2d Supp. Br. re: Technical Aspects of Accused Products, Docket No. 185 at 1 ("CCCC Supp. Br. II") ("[A] SNOOP signal indicates whether an address falls within a range of addresses subject to caching – i.e., a cache

data storage location"). The primary distinction between the parties' interpretations of the court's construction involves whether the SNOOP signal indicates the absence or presence of cached data at the referenced location. Neither party contends that the SNOOP signal indicates whether the data is coherent or not – the disagreement is over whether the SNOOP signal indicates that data has been cached for an address or whether the SNOOP signal only indicates whether an address is capable of being cached (or "cacheable").

The parties agree that the VIA and Intel chipsets originally accused by CCCC of infringing the '369 patent do not assert a SNOOP signal that indicates whether an address is one that is in cache. CCCC Supp. Br. II at 1-2. Thus, if the court's construction means what defendants argue it does, none of Intel's originally-accused products can be found to literally infringe the '369 patent.

CCCC's proposed construction suggests that the claimed "SNOOP signal" has no knowledge of whether the data at the referenced address is cached but merely "trigger[s] a determination" of whether the data at a referenced location is cached. In its claim construction order, the court rejected CCCC's proposed construction, stating "the SNOOP signal indicates whether an address references a cached storage location, it does not merely trigger a determination whether data is cached." Claim Construction Order at 12. CCCC's interpretation of the court's construction of SNOOP signal – that the SNOOP signal indicates whether the address is one that is cacheable – is consistent with its proposed construction, previously rejected by the court. *See, e.g.*, 8/20/02 Expert Hearing Tr. 43:1-45:2 (Dubois testimony regarding his understanding of the meaning of "cached" prior to and after the court's claim construction order).

b. Bus Snooping

As a background to understanding the nature of a snoop operation, CCCC explains bus snooping as follows: In a system wherein data is cached,[4] main memory and cache memory both store data. Decl. Michael Dubois Supp. of CCCC Supp. Br. II ("Dubois Supp. II Decl.") ¶ 9. The main memory and cache memory addresses are mapped to each other such that an address may refer

[4] In a cache-based system, some areas of memory are cached while other areas of memory are not cached. Dubois Supp. Br. II Decl. ¶ 15.

to either an address in main memory or a corresponding address in cache memory. *Id.* If the data in the main memory is not the same as the data in cache memory, the data is non-coherent. *Id.* ¶ 10.

According to CCCC, "bus snooping" is a method for solving the cache coherency problem. *Id.* ¶ 12. In a single bus configuration, "bus snooping" occurs when processor seeking to read from or write to an address that may be cached puts the operation on hold in order to determine whether a coherency problem exists and, if so, to resolve it. *Id.* In bus snooping, a snoop cycle is initiated by a signal or request (called a "SNOOP signal") being asserted on the bus for the address from which the processor seeks to read or to which the processor seeks to write. *Id.* ¶ 14. The SNOOP signal initiates the process for determining whether a coherency problem exists. *Id.* ¶ 12. CCCC contends that at the time of the invention in 1989, the inventors would have understood that a SNOOP signal is asserted whenever a processor seeks to read from an address falling with a range of addresses corresponding to the range of addresses accessible by cache memory or, in other words, an address that is cacheable. *Id.* ¶ 14, 19, 21.

c. CCCC's Supplemental Argument

CCCC asserts that the SNOOP signal described in the '369 patent operates in the manner described above such that it is asserted whenever the processor seeks to read from any address that is cacheable. *Id.* ¶ 19. In short, CCCC contends that the SNOOP signal claimed in the '369 patent is no different from any other SNOOP signal in that it merely seeks to determine whether data at a cached address is non-coherent. It points to a passage of the '369 patent that describes the functionality of the SNOOP signal in a single cache environment in support of the contention that nothing more than an ordinary SNOOP signal is claimed in claim 1. *See* Dubois Supp. II Decl. ¶ 20 (citing the description of SNOOP signal in connection with the Futurebus at lines 36-52 of the '369 patent).

According to CCCC, a person of skill in the art in 1989 would have understood that a SNOOP signal was incapable of indicating whether or not data was in the cache and that a data tracking feature would have been novel. CCCC Supp. Br. II at 1; Dubois Supp. II Decl. ¶ 21. In particular, CCCC contends that when the SNOOP signal is asserted by the interface circuit for an address, the interface circuit has no knowledge of whether data is being held in cache for that

address. CCCC Supp. Br. I at 4. CCCC asserts that because the processor ("bus master") connected to the second bus is caching data, only that processor/bus master, not the interface circuit, can know when data moves in and out of the cache. Specifically, CCCC argues that only the processor and not the SNOOP signal can know when data moves in and out of a cached data storage location because claim 1 requires the bus interface circuit to "generate a SNOOP signal of a state indicating when a generated second address is mapped to one of said particular subset of the second data storage locations."[5] CCCC Supp. Br. I at 4.

CCCC points to the following passage in the specification that describes the function of the SNOOP signal in the context of the invention in support of its position that the claimed SNOOP signal does not have any knowledge regarding whether the data at the referenced storage location is cached:

> When a computer processor on the VMEbus attempts to read or write access any one of the set of VMEbus addresses, the mapping circuit generates a corresponding Futurebus address and a SNOOP signal indicating whether the Futurebus address references a cached data storage location on the Futurebus. The bus interface circuit then obtains control of the Futurebus and starts a read or write access cycle by placing the SNOOP signal and the generated address on the Futurebus. ***If the SNOOP signal indicates the Futurebus address references a cached data storage location, another computer processor on the Futurebus controlling the cache responds to the SNOOP signal with a retry signal.*** The bus interface circuit then relinquishes control of the Futurebus to the other computer processor to permit the other computer processor to write data from the cache into the storage location referenced by the generated Futurebus address. Thereafter, the interface circuit regains control of the Futurebus and completes a read or write access of that data storage location.

'369 patent at 2:20-30 (emphasis added). CCCC acknowledges that Intel and Via point to the emphasized language as supporting their contention that the SNOOP signal indicates that cached data resides in cache memory. Dubois Supp. II Decl. ¶ 22. The contention is based upon the fact that the sentence states implies that every time the SNOOP signal indicates that an address references a "cached data storage location," the processor controlling the cache responds with a retry signal. If so, the "cached data storage location" is not one that is merely cacheable, but instead the SNOOP signal knows that the data storage location is in cache and thus will always assert the retry signal. The parties agree that there would be no need to assert the retry signal if the data storage location were not cached. Nevertheless, CCCC asserts that "while one may understand this sentence

[5] The parties agree that "subset of the second data storage locations" refers to the cache memory.

to mean that the processor with a cache always responds to the SNOOP signal with a retry, a person of ordinary skill in the art would not understand the sentence in this manner, because it would be inconsistent with other discussions in the '369 patent specification regarding the 'SNOOP signal.'" *Id.* CCCC suggests that such a person would read the word "may" into this sentence (i.e., "If the SNOOP signal indicates the Futurebus address references a cached data storage location, another computer processor on the Futurebus controlling the cache **[may]** respond**[]** to the SNOOP signal with a retry signal."). This, CCCC contends, would comport with its interpretation that the SNOOP signal only indicates that a data storage location is cacheable because it allows for the retry signal to only respond with a retry to the SNOOP signal when the location is cached, rather than always responding to the SNOOP signal when the location is only cacheable (which would be nonsensical). The question, however, is whether at the time and based upon other information in the claim and specification, a person of ordinary skill in the art would have necessarily have read "may" into the subject sentence.

d. Intel and Via's "SNOOP Signal" Interpretation

As set forth above, Intel and Via's interpretation of the court's construction of SNOOP signal requires the SNOOP signal to indicate when data is actually in cache rather than just trigger a determination of whether data is in cache. To be clear, according to Intel and Via, the SNOOP signal need not know whether the data is coherent or not, only that the address referenced is one that is in cache. Intel's expert, Dr. Levy, explained that a way to implement this functionality (which he acknowledged was not normally part of the SNOOP operation in a static system) was a "lock and load" mechanism. Dr. Levy characterized the lock and load mechanism as a well known software solution for tracking the movement of data in and out of the cache:

> Well, there are mechanisms by which software can also force certain things to remain in cache rather than being brought in and out automatically. They come in automatically, but there is a well known mechanism called load and lock for caches in which data is brought in, as it describes in column 9 of the patent, a block of data is brought into the cache and it remains there until the software decides to unlock it and release it.
>
> And so in that case, the interface circuit, with its snoop bit, could, in fact, know, or have a snoop bit of a state that indicates whether data is actually in cache.

8/20/08 Expert Hearing Tr. 14:2-15. Dr. Levy was, however, unable to point to any description in the '369 specification of the lock and load software mechanism. *Id.* at 49:5-8 ("Mr. Hadley: "[I]s

there anything in the Specification that expressly describes this load and lock software mechanism that you explained? Mr. Levy: No."). Nor was he able to point to anything in the specification that limits the invention to systems that existed at the time the patent application was filed that had a lock and load mechanism. *Id.* at 49:9-22. Nor did Dr. Levy seriously contend that such a mechanism was understood to be part of a snoop operation at the time of the invention. Thus, the court must carefully review the language of the claim in light of the specification to insure that it does not read a limitation on SNOOP signal that is not claimed.

The description of the SNOOP signal in the context of the invention, however, rather clearly indicates that the claimed SNOOP signal understands which addresses in memory contain cached data. For example, the '369 patent abstract sets forth that "[t]he bus interface circuit stores SNOOP data indicating which memory addresses contain data cached in the cache memory" and when a bus master on the first bus seeks to access a cached memory address, "the bus interface circuit places a signal on the second bus telling the second bus master to copy data from the cache memory into the main memory." '369 patent at 1.

Additionally, claim 1 strongly indicates that the SNOOP signal understands which addresses are in cache. The specification explains that when the bus master on the first bus attempts to access mapped addresses on the first bus "the mapping circuit generates a corresponding [address on the second bus] and a SNOOP signal indicating whether [the address on the second bus] references a cached data storage location on the [second bus]." *Id.* at 12:7-13. In claim 1, this signal placed by the bus interface circuit is claimed as "the SNOOP signal telling one of said second plurality of bus masters when to write cached data to the address appearing on the bus," *id.* at 13:11-14, demonstrating that when the interface circuit asserts a SNOOP signal, the circuit knows whether an address requested by the first bus is mapped to an address on the second bus that contains data cached in the cache memory. The '369 patent specifies that the claimed mapping means generates a SNOOP signal only when the address on the second bus "is mapped to one of said particular subset of the second data storage locations." '369 patent at 14:1-2.

Thus, as claimed, the SNOOP signal is only asserted by the interface device when an address maps to an address on the second bus at which data is known to be cached. Accordingly, the court

confirms that under its construction of the term ("a signal indicating whether an address references a cached data storage location"), the SNOOP signal must indicate that data is cached at the referenced location. The court has some reservations about this construction since, as discussed above, the specification does not seem to indicate how the interface data would know that an address has been cached. Nevertheless, the language in the abstract and claim clearly suggests that the claimed interface circuit knows and asserts a SNOOP signal only for addresses that are cached. Further, if after the reasoned analysis set forth above, both interpretations are equally plausible, the patentee's statutory burden to distinctly claim subject matter favors the narrower construction. *See Athletic Alternatives, Inc. v. Prince Mfg., Inc.*, 73 F.3d 1573, 1581 (Fed. Cir. 1996).

4. SNOOP Signals in Intel's Accused Products

Claim 1 of the '369 patent requires that the second bus, include a "means for conveying a SNOOP signal with an address appearing on the bus." '369 patent at 13:9-10. CCCC argues that the accused chipsets of both Intel and Via incorporate a cache coherency protocol that infringes the '369 patent because the protocol initiates a snoop cycle utilizing a SNOOP signal. As discussed above, the court has concluded that the claimed "SNOOP signal" must indicate whether data is cached at the referenced location. As agreed by the parties and discussed below, the result of the court's construction means that the Via and Intel accused products that do not implement a snoop filter do not infringe claim 1 of the '369 patent.

a. HREQ [4:0]

CCCC contends that Intel and Via chipsets initiate the snoop cycle by placing the requested address on the FSB[6] along with the requested information. It asserts that this address and requested information is the SNOOP signal because the "request cycle contains information sufficient for the processor to perform the SNOOP lookup" and the FSB responds to this request cycle by determining if its cache memory is holding the data at the requested address and if that data has been modified since it was taken from main memory. CCCC Supp. Br. II at 7.

[6] The FSB or front side bus connects the processor to the Northbridge (known as the MCH in Intel's chipset).

Intel argues that it cannot infringe claim 1 because CCCC has only identified an address that is asserted on the front side bus but has failed to identify a separate SNOOP signal that accompanies the address. CCCC, on the other hand, points to a "request cycle" that is initiated on the front side bus and contends that the request cycle is a SNOOP signal. Specifically, CCCC asserts that Intel's chipsets place on the front side bus a signal comprised of an address and a request. The address makes up 32 bits of the signal and specifies where the requested data is located, while a 4-bit request signal portion, HREQ[4:0], specifies what sort of operation is to be performed. In its opposition to Intel's motion for summary judgment and in supplemental briefing, CCCC reiterates its contention that these 4 bits, the HREQ[4:0] signals generated by the Northbridge, are a SNOOP signal according to the court's construction.[7]

To illustrate, the Intel 925X Express Chipset Design Specification ("925X Specification") describes HREQ[4:0] as the "Host Request Command," which defines the attributes of a request. The HREQ[4:0] signal is the 4-bit signal that indicates what type of operation, i.e., read or write, is to be performed at the requested address. Rabe Dep. at 105:20-106:2. According to the 925X Specification, the HREQ[4:0] are signals asserted by requesting agent "during both halves of the Request Phase." *See* Salik Decl. Supp. MSJ v. Intel, Ex. 1, 925X Specification at 23.

CCCC states "there is no dispute that the HREQ signal *is a signal that begins a Snoop transaction*." CCCC Supp. Br. re: MSJs, Docket No. 139-2 at 3 (emphasis added); *see also* CCCC

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[7] Intel asserts that CCCC's preliminary infringement contentions stated only that the presentation of the address to the processor through the front side bus, and that CCCC's present position is an impermissible attempt to amend its preliminary infringement contentions. The court disagrees. CCCC's preliminary infringement contentions state:

> A SNOOP bus cycle is performed when, for example, a PCI bus master attempt to access main memory. If the 82443GX determines that a SNOOP cycle is required, the HREQ[4:0]# lines assert a Request Command. . . . In a SNOOP cycle, the 82443GX places the memory address on the Front Side bus so it can be tested by the Pentium II processor. The Pentium II processor monitors the memory addresses appearing on the Front Side bus. If a main memory address on the Front Side bus matches the address of data that has been cached by the processor, the processor will generate a HIT# signal to the 82443GX. If the data in cache has been modified by the processor since it was read out of main memory, the processor will generate the HITM# to the 82443GX. A HIT# or HITM# will cause the 82443GX to abort the memory access request. This presentation of the address to the Pentium II on the Front Side bus is a SNOOP signal.

Decl. John Farrell Supp. Intel's Opp'n CCCC's MSJ Infringement, Ex. 2 at 6-7. The court finds CCCC's preliminary infringement contention sets forth its position that the Request Command asserted on the HREQ[4:0]# lines are the SNOOP signal.

Supp. Br. II at 8 ("Once asserted, the HREQ signal begins a Snoop transaction."). Indeed, according to the 925X Specification, the HREQ[4:0] signals "define the transaction type to a level of detail that is sufficient to begin a snoop request." Salik Decl. Supp. MSJ v. Intel, Ex. 1, 925X Specification at 23. In response to receiving the HREQ[4:0] signals from the Northbridge of the accused chipsets, the processor (which is not a component of the accused chipsets) will assert snoop cycle signals HIT# and HITM# to indicate whether data resides at the cached location requested[8], and will return signals indicating to the Northbridge whether the data corresponding to the address is in cache and has been modified. *See, e.g.*, Rabe Dep. at 110:2-13; 111:12-112:15.

However, merely triggering a determination of whether data is cached at the location corresponding to the mapped address is not enough to meet the SNOOP signal limitation. As clarified by the discussion above, the SNOOP signal must also do more than indicate that an address is cacheable. The interface circuit claimed in the '369 patent requires the circuit to know that the address it has mapped to the second bus has cached data in a corresponding cache location. Thus, the SNOOP signal generated by the mapping means of the claimed apparatus must indicate whether there is data in cache that corresponds to the mapped address on the second bus.

That the claimed interface circuit knows that the address it has mapped has associated cached data is further evidenced by the requirement set forth in claim 1 that the mapping means generate "a SNOOP signal of a state indicating when a generated second address is mapped to one of said particular subset of the second data storage locations." It is undisputed that the HREQ[4:0] signals that are asserted by the Northbridge do not indicate whether there is data at the corresponding address in cache on the second bus. When the MCH places the HREQ signal on the FSB, it does not know whether the data at the corresponding address is cached or not, thus the HREQ signals do not indicate whether the data corresponding to the address is cached, although these signals do appear to trigger such a determination once they are received by the processor. The court thus concludes that there can be no literal infringement of the '369 patent because the accused Intel chipsets do not assert a SNOOP signal as required by claim 1.

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[8] The HIT# signal indicates that a snoop resulted in seeing data in cache that was not modified. HITM# indicates that a snoop resulted in seeing data in the cache that has been modified. Rabe Dep. 117:24-118:5.

In a footnote, Intel acknowledges that the DMI, which connects the Northbridge to the Southbridge in some of Intel's chipsets, may assert a "no snoop required" bit. *See* Intel's Opp'n to CCCC's MSJ re: Literal Infringement at 5 n.4. This bit appears to only be asserted between the Northbridge and Southbridge of the Intel chipsets that utilize a DMI connection (other chipsets utilize a hub link interface or HI rather than a DMI). Rabe Dep. at 94:7-95:12. CCCC presents no evidence that this "no snoop required" bit is ever asserted on the front side bus and there is no contention that the DMI connection linking the Northbridge to the Southbridge is one of the two busses described in the preamble of claim 1. Thus, the "no snoop required" bit does not meet the "SNOOP signal" limitation of claim 1.

With respect to the doctrine of equivalents, CCCC does not present "particularized testimony of a person of ordinary skill in the art" suggesting that Intel's accused chipsets include the equivalent of a SNOOP signal as required by claim 1. *AquaTex Industries, Inc. v. Techniche Solutions*, 479 F. 3d 1320,1329 (Fed. Cir. 2007). Therefore, Intel's motion for summary judgment under the doctrine of equivalents is also granted.

b. Snoop Filter

A "snoop filter" is a structure included in a chipset that is designed to reduce the number of snoop signals asserted on the FSB. A snoop filter is "essentially a table that keeps track of all the data that moves in and out of the processor's cache memory." CCCC Supp. Br. II at 9. Neither defendant appears to dispute this characterization of the snoop filter.

According to CCCC, in Intel's products that include a snoop filter,[9] a request from a PCI device is received into a unit of the chipset called the "coherency engine and data manager." This coherency engine performs the "snoop filter lookup," whereby the chipset checks the snoop filter table to determine if the address requested by the PCI device corresponds to data that has (or has not) been placed in a cache memory of one or more of the processors. Based on the result of the snoop filter lookup, the coherency engine determines whether to initiate a snoop cycle on the FSB. If the snoop filter lookup results in a determination that the requested data has not been placed in

[9] Intel acknowledges that one of the 64 originally-accused chipsets, the E8870, includes a snoop filter. It asserts that of the 38 new chipsets CCC seeks to add, only three – the 5000x (Green Creek), the 5400 (Seaburg) and the 7300 (Clarksburo) – include a snoop filter.

cache memory in any of the processors, no snoop inquiry is performed because there is no coherency problem. If the snoop filter lookup results in a determination that the requested data has been placed in the cache, the processor transmits the updated data to the chipset to complete the read.

Intel does not appear to dispute that the snoop filter fulfills the function of the SNOOP signal as construed by the court. Rather, Intel contends that its products including a snoop filter do not meet the following limitation of claim 1: "the SNOOP signal telling said one of said second plurality of bus masters when to write cached data to the address appearing on the bus." This contention is discussed in the following "Snoop Signal Telling."

5. "SNOOP Signal Telling"

Assuming either that the correct construction of SNOOP signal is that the signal indicates whether an address references a cacheable data location as CCCC proposed, or that the presence of a snoop filter means that an accused product meets the SNOOP signal limitation, the Intel products still do not infringe claim 1 of the '369 patent.

a. The Chipsets Do Not "Tell"

The court construed "the SNOOP signal telling one of said second plurality of bus masters when to write cached data to the address appearing on the bus" as "the SNOOP signal indicating to one of the bus masters on the second bus when to write cached data to the one of the second data storage locations at the address appearing on the second bus." This construction requires the SNOOP signal to indicate to a device on the second bus that it should write data held in that device's cache memory to main memory on the second bus.

Intel asserts that its chipsets do not infringe claim 1 of the '369 patent because they fail to meet this limitation. First, Intel asserts that the HREQ signals that CCCC asserts are the SNOOP signal do not tell the processor when to write data to main memory. Instead, if the processor determines in response to an HREQ signal that it has the data in its cache and the data has been modified, the processor places a HITM# signal on the FSB; if there is data in the cache and the data has not been modified, the processor places a HIT# signal on the FSB. The chipset – specifically the Northbridge (MCH) – will then assert a TRDY signal to tell the processor to place the modified data on the FSB. Thus, it is the TRDY signal, not the HREQ signal, that tells the "bus master on the

second bus" (the processor) when to write cached data. CCCC does not contend that the TRDY signal is the SNOOP signal, and Intel asserts that such an argument would be futile, since claim 1 requires the SNOOP signal to be asserted along with an address and it is undisputed that no address accompanies the TRDY signal. The HIT#/HITM# signals cannot meet the "SNOOP signal telling" claimed in the '369 patent because they are asserted by the processor rather than by the chipset.

According to Intel, this HREQ/HITM/TRDY sequence is also performed in the chipsets that include a snoop filter and therefore the chipsets implementing a snoop filter likewise do not meet the "SNOOP signal telling . . ." limitation. CCCC's argument to the contrary is no convincing.

The court concludes that Intel's chipsets cannot literally meet the "SNOOP signal telling" limitation because it does not appear that the HREQ signal "indicates to a device on the second bus that it should write data held in that device's cache memory to main memory on the second bus." Nor does it appear that CCCC would be able to prove that the "SNOOP signal telling" limitation could be met under the doctrine of equivalents given that there is no evidence or argument that any other signal or set of signals that are asserted by the chipset function in the same way to obtain the result claimed. *See AquaTex Industries*, 479 F. 3d at1329 (reliance on the doctrine of equivalents requires "particularized testimony of a person of ordinary skill in the art, typically a qualified expert, who . . . establishes that those skilled in the art would recognize the equivalents.)

b. Devices on the Chipset Do Not Write to Main Memory

Second, Intel asserts that the devices on the chipset do not write cached data to main memory. Rather, Intel's chipsets hold data in a global write buffer ("GWB") that is part of the Northbridge (MCH). Rabe Decl. ¶ 14. From there, an internal chipset signal, the TRDY signal, directs the Northbridge (MCH) to write the data from the GWB to main memory. While the data is being held in the GWB, another device may provide the Northbridge with the data intended for the address corresponding to the previously cached data. If this happens, the Northbridge will overwrite the cached data stored in the GWB and the data that was written to the GWB as a result of the HREQ signals will never be written into main memory. Because the HREQ signal only results in data being written to the GWB and it is the TRDY signal that signals the GWB to write to main memory, it does not appear that the Intel chipsets exhibit the required behavior of directing devices

to write cached data into main memory. As discussed above, it would appear that the TRDY signal generated by the processor (and not the chipset) directs writing to main memory.[10]

C. Alleged Infringement by Via

1. CCCC's Infringement Contentions

CCCC contends that it should be granted summary judgment that the accused Via chipsets infringe the '369 patent. CCCC asserts that the Via chipsets meet every limitation of claim 1 of the '369 patent. Via, on the other hand, argues that its products do not infringe because Via's accused chipsets do not include a "bus" meeting the court's construction. Like Intel, Via also argues that its accused chipsets do not assert a SNOOP signal as required by claim 1.[11]

2. First and Second Buses

As with the Intel chipsets, CCCC asserts that the first bus limitation is met by a PCI bus connected to the accused Via chipsets. It asserts that the front side bus ("FSB") in the Via chipsets is the second bus. Via, pointing out that its chipsets are designed for use in computer systems with Intel and AMD processors, contends that its accused chipsets do not themselves include a first bus or a second bus as required by the preamble of claim 1 and thus cannot directly infringe the '369 patent. As discussed above, the court has concluded that the accused chipsets need not themselves include the first and second buses as described in the preamble, rather must provide the claimed apparatus that operates in the environment described in the preamble. Therefore, CCCC's infringement theories are not, as Via argues, limited to inducement and contributory infringement. Next, Via contends that its chipsets do not include a first address space and second address space as required in

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[10] Intel also presents a non-infringement argument based upon a limitation the court determined it did not need to construe because it should be construed according to its plain meaning: "receiving data from a second data storage location mapped to second address." Intel argues that the claim requires the bus interface means to "receiv[e] data from a second data storage location mapped to said second address," or that when the chipset writes data to a device, that the data to be written to the device be received from main memory (the "second data storage location"). According to Intel, in its chipsets the data is received from the cache, not from main memory. Because the court has determined that Intel's chipsets do not meet the "SNOOP signal telling" limitation, the court need not reach this argument.

[11] Via also argues that statements made during the prosecution of U.S. Patent No. 5,088,028 should be used to limit the scope of the '369 patent. The application for the '369 patent and the parent application of the '028 patent were both filed on April 7, 1989, but were not formally related. The court does not consider this argument as CCCC does not move for summary judgment of infringement under the doctrine of equivalents.

the preamble. The court construed "first address space" to be an address space that necessarily refers to addresses represented on the first bus and a "second address space" to be an address space that necessarily refers to addresses represented on the second bus. According to Via, CCCC's infringement theory is that main memory constitutes both the first and second address space. Via asserts that a single memory cannot meet the requirement for both a first and second address space. It appears that Via's chipsets utilize a global address space that is shared by numerous devices rather than having an entirely separate address space for each bus. However, the court cannot determine based on the evidence presented whether global address space includes a range of addresses that refers to addresses on the PCI bus that is separate from a range of addresses that refers to addresses on the front side bus. Accordingly, there appears to be a question of fact whether the address space limitations are present in the accused Via chipsets.

Finally, Via argues that CCCC has failed to prove a "second bus" meeting the limitations set forth in the second paragraph of the preamble. As discussed above, the court's construction of bus requires the bus to be more than a point-to-point bus that connects only two devices in light of the express language in the preamble requiring a "plurality of bus masters" on each of the buses. CCCC asserts that the front side bus connecting the Northbridge of the Via chipsets to the processor is the second bus. The only evidence before the court, however, is that in the Via chipsets the front side bus connects only the Northbridge to the processor – there is no evidence that any other device connects to the front side bus. Although CCCC argues that the front side bus is capable of supporting multiple bus masters, it presents no evidence that the front side bus in the Via chipsets actually does so. Further, Via presents evidence that in its K8 chipsets, the main memory is connected directly to the K8 processor and does not connect to the Northbridge at all. Although CCCC argues that Via has failed to present evidence that the front side bus in the K8 chipsets do not include the limitations required of the second bus, it is not Via's burden to do so. Accordingly, there appears, at minimum, to be a question of fact whether Via's chipsets operate with a second bus that meets the limitations of the second paragraph of the preamble.

3. SNOOP Signal

a. ATTR

Via, like Intel, asserts that its accused chipsets do not include a SNOOP signal as construed by the court. Relying on its proposed construction that a SNOOP signal need only "trigger a determination of whether the data corresponding to an address in cacheable memory is cached," CCCC argues that the ATTR[7:0] signal asserted by the Northbridge chip on the front side bus along with the address is the required SNOOP signal. However, as discussed above, the court has determined that the SNOOP signal generated by the mapping means of the claimed apparatus must indicate whether there is data in cache that corresponds to the mapped address on the second bus. As with the HREQ[4:0] signal discussed above, CCCC presents evidence that the ATTR[7:0] signal indicates whether an address is cacheable. While the information regarding whether an address is cacheable may be sufficient to trigger the processor to perform a snoop operation on the cache, however, CCCC does not provide any evidence that the ATTR[7:0] signal asserted by the Northbridge indicates whether there is data at the corresponding address in cache on the second bus. *See* Peuto Decl. ¶ 59 (the Northbridge does not have access to information permitting it to determine whether an address it will place on the front side bus refers to a data storage location which has actually been cached as only the cache itself can determine whether a particular data storage location in the cache is in fact cached). The court concludes there can be no literal infringement of the '369 patent based on the argument the ATTR[7:0] is a SNOOP signal, because, as construed, the SNOOP signal must do more than trigger a determination that data is cached.

b. HIT and HITM

CCCC next asserts that the HIT and HITM signals that are conveyed from the processor to the Northbridge are the required SNOOP signal. Via argues that the HIT and HITM signals cannot be the SNOOP signal for two reasons: (1) the HIT signal does not indicate that data has been modified and thus cannot be the SNOOP signal; and (2) neither HIT or HITM is generated by the chipset, and thus cannot be the claimed SNOOP signal.[12] Via's first argument is without merit. Although the HIT signal may not indicate that data has been modified, it is undisputed that HITM is

[12] At the supplemental expert hearing on August 20, 2008, Intel presented similar arguments on its own behalf.

conveyed when the cache data has been modified. As it appears that either HIT or HITM is asserted such that the absence of HITM would indicate that the data has not been modified.

It does, however, appear that Via is correct that HITM is not generated by the first mapping means as required by the language of claim 1. Because HIT and HITM are generated by the processor rather than the chipset, these signals cannot literally meet the SNOOP signal limitation, since the first mapping means must generate a SNOOP signal.

c. Snoop Filter

Following the court's issuance of its claim construction order, CCCC submitted a motion to dismiss or stay Via's motion for summary judgment of non-infringement pursuant Rule 56(f), asserting that it had recently determined that Via's chipsets may include a feature called a "snoop filter" operating in a manner consistent with the court's construction of "SNOOP signal."[13] CCCC sought and was granted permission to seek additional discovery to determine whether Via's chipsets include this feature and how the feature operates. CCCC asserts, without support, that Via's chipsets support snoop filtering; Via asserts, pointing to the testimony of its designated witness, J.S. Sheu, that the accused chipsets do not support snoop filtering. Evidently, the parties dispute whether the witness designated by Via has sufficient knowledge regarding this feature and have filed a motion to compel. Accordingly, the court is unable to determine at this time whether the accused Via chipsets implement snoop filtering. Nevertheless, for the reasons set forth above with respect to the accused Intel chipsets, the court concludes that the "SNOOP signal telling" limitation is not met and thus Via's chipsets do not infringe claim 1 of the '369 patent.

d. HREQ

Although it has not been clear to the court in previous rounds of briefing, it appears that CCCC also asserts that the HREQ[4:0] signal in the Via chipsets is the required SNOOP signal. The

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[13] Rule 56(f) provides:

> If a party opposing the motion shows by affidavit that, for specified reasons, it cannot present facts essential to justify its opposition, the court may:
> (1) deny the motion;
> (2) order a continuance to enable affidavits to be obtained, depositions to be taken, or other discovery to be undertaken; or
> (3) issue any other just order.

contention that HREQ is the SNOOP signal in the Via chipsets suffers from the same infirmities as the contention in the context of the Intel chipsets and for the same reason the court finds that HREQ is not the required SNOOP signal.

4. "SNOOP Signal Telling"

The discussion above regarding whether the Intel chipsets can meet the "SNOOP signal telling" limitation applies equally to the Via chipsets. Accordingly, the court finds that CCCC has failed to present evidence that the VIA chipsets practice the "SNOOP signal telling" limitation and that the accused products can thus not literally infringe the patent.

5. Via's Motion for Partial Summary Judgment of Non-Infringement Based on the AMD License and Notice Dates

As set forth above, Via's accused chipsets operate with processors made by Intel and AMD.[14] CCCC sued AMD in this court on April 25, 2005 (the same date it sued Intel in Case No. 05-01766-RMW). *CCCC v. AMD*, Case No. 05-01767-RMW. On September 29, 2005, CCCC and AMD entered into a Settlement and License Agreement regarding the '369 patent. CCCC and AMD agreed to settle the matter for a paid up royalty of $200,000 for past, present, and future use by AMD of the '369 patent. Decl. Murray Levi Supp. Via's Mot. Summ. J. Non-infringement, Ex. A at 3 ¶¶ 2.1, 3.1. CCCC further covenanted not to sue AMD customers, distributors and users of "Licensed Products" as defined by that Settlement Agreement. *Id.* ¶ 4.1. On September 30, 2005, CCCC and AMD filed a stipulation to dismiss Case No. 05-01767-RMW without prejudice.[15]

Based on its argument that Via must supply the first and second buses as set forth in the preamble in order for any of its chipsets to infringe the '369 patent, Via moved for partial summary judgment as to the AMD-compatible chipsets. Specifically, Via contends that the covenant not to sue AMD customers set forth in the Settlement Agreement between CCCC and AMD precludes a finding that Via infringes the '369 patent. According to Via, if it cannot directly infringe because the

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[14] The accused Via chipsets that work with AMD's processors are: K8T890, K8T900, K8T800 (AMD's K8 processor); and KT600, KT880, KM400A, KT400, KT400A, KT133, KT133A, KX133, KT266, KT266A (AMD's K7 processor). Decl. Jennifer Ochs Supp. Via's Mots. Summ. J. ("Ochs Decl.") ¶ 12. A Via K8 chipset can only be used in combination with an AMD K8 processor; a Via K7 chipset can only be used in combination with an AMD K7 processor. Peuto Decl. ¶ 46.

[15] The court entered its order on the parties' stipulation and closed the case on October 5, 2005.

preamble requires it to supply the first and second buses set forth in the preamble, CCCC is necessarily limited to asserting only indirect infringement theories (contributory infringement and indirect infringement). Contributory infringement and indirect infringement both require some showing of direct infringement. *Carborundum Co. v. Molten Metal Equip. Innovations, Inc.*, 72 F.3d 872, 876 n.4 (Fed. Cir. 1995) ("Absent direct infringement of the claims of a patent, there can be neither contributory infringement nor inducement of infringement."). Based on its position regarding the limiting effect of the preamble, Via argues that AMD-compatible chipsets can only be found to directly infringe when combined with AMD processors by AMD, its customers, distributors and users. It further argues that because CCCC has granted a license to AMD and has covenanted not to sue AMD's customers, distributors and users, there can be no liability for direct infringement with respect to AMD-compatible chipsets.

A few weeks after Via filed the instant motion for summary judgment, CCCC and AMD revised the terms of the Settlement Agreement, entering into the First Amended and Restated Settlement and License Agreement, dated as of September 29, 2005. *See* Decl. Lawrence Hadley ("Hadley Decl."), Ex. 1. The Revised Settlement Agreement narrowed the scope of the release.

In the briefing on Via's motion, the parties dispute many issues, including (1) the applicability of the patent exhaustion doctrine, recently discussed in *Quanta Computer, Inc. v. LG Electronics, Inc.*, ___ U.S. ___; 128 S.Ct. 2109 (2008); (2) and the impact of the amendment of the Settlement Agreement by CCCC and AMD. However, Via's argument starts with the proposition that it can only be liable for indirect infringement. As set forth above, the preamble does, indeed, provide limitations to claim 1 and Via may not be found to infringe the '369 patent unless CCCC can prove that Via's chipsets operate in the environment set forth in the preamble. Nevertheless, as discussed above, Via's accused AMD-compatible chipsets need not supply the first and second buses in order to directly infringe, such that CCCC's infringement theories are not, as Via argues, limited to inducement and contributory infringement. Thus, because Via may be found to directly infringe the '369 patent without resort to indirect infringement liability, the court must deny Via's motion for summary judgment of non-infringement to the extent it is based on the AMD license and notice dates.

D. Invalidity

Based on CCCC's proposed claim constructions, Intel moves for summary judgment that the '369 patent is invalid as anticipated or obvious in light of two references it refers to as "the Clipper System" and "the Sequent Multiprocessor System." Intel asserts that two references, a document titled "Clipper C300 32-Bit Compute Engine Data Sheet" by Intergraph ("the Clipper datasheet") and an article authored by Frank Hart, titled "Adapter circuit marries RISC to a PC-AT and other buses" ("the Hart article"), together form a single prior art reference which it refers to as "the Clipper System." Similarly, Intel asserts that two publications, an article by Tom Lovett, et al., titled "The Symmetry Multiprocessor System" ("the Lovett article") and an article titled "The Balance Microprocessor System" by Shreekan Thakkar, et al. ("the Thakkar article") together form a single prior art reference which Intel refers to as the "Symmetry System."[16]

Based on the fact that it adopted claim constructions that are different from those proposed by CCCC, the court is unable to accurately assess Intel's invalidity arguments. As a result, it cannot state as a matter of law that no material facts remain as to whether either the Clipper System or the Symmetry Multiprocessor System either anticipate or render obvious the '369 patent. It therefore denies Intel's motion for summary judgment of invalidity without prejudice.

[16] For purposes of this motion, the court need not decide whether Intel properly refers to these "systems" as a single prior art reference for purposes of its anticipation argument.

United States District Court
For the Northern District of California

III. ORDER

For the reasons set forth above, the court rules on the pending motions as follows:

1. CCCC's motion for summary judgment of infringement against Intel is denied. (Case No. 05-01766, Docket No. 76);
2. CCCC's motion for summary judgment of infringement against Via is denied. (Case No. 05-01668, Docket No. 109);
3. Via's motion for summary judgment of non-infringement to the extent that it is based on the AMD License and Notice Dates is denied. (05-01668, Docket No. 101);
4. Via's motion for summary judgment of non-infringement is otherwise granted. (Case No. 05-01668, Docket No. 107);
5. Intel's motion for summary judgment of non-infringement is granted. (Case No. 05-01668, Docket No. 96);
6. CCCC's motion to amend to add new Intel products is denied as amendment would be futile. (Case No. 05-01766, Docket No. 150); and
7. Intel's motion for summary judgment that the '369 patent is invalid as anticipated or obvious is denied without prejudice. (Case No. 05-01668, Docket No. 105)

DATED: 09/19/08

Ronald M. Whyte
RONALD M. WHYTE
United States District Judge

Notice of this document has been electronically sent to:

Counsel for Plaintiff:

Roderick G. Dorman	dormanr@hbdlawyers.com
Lawrence M. Hadley	hadleyl@hbdlawyers.com
Omer Salik	saliko@hbdlawyers.com

Counsel for Defendants:

James P. Bennett	jbennett@mofo.com
Juanita R. Brooks	brooks@fr.com
Joseph V Colaianni , Jr	Colaianni@fr.com
Paul Forrest Coyne	pcoyne@mofo.com
John Michael Farrell	jfarrell@fr.com
Karl J. Kramer	kkramer@mofo.com
Jennifer A. Ochs	jochs@wsgr.com
Timothy Wayne Riffe	Riffe@fr.com

Counsel are responsible for distributing copies of this document to co-counsel that have not registered for e-filing under the court's CM/ECF program.

Dated: 09/23/08

JAS
Chambers of Judge Whyte

United States District Court
For the Northern District of California